number of host applications and providing result/status information to the number of host applications; and

A1 and

control logic operably coupled to obtain memory access requests from the number of contexts, interact with the memory device over the memory interface for servicing the memory access requests on behalf of the number of host applications in accordance with the interface requirements for the memory device, and provide the result/status information to the number of host applications via the number of contexts in accordance with the interface requirements for each of the number of host applications.

A2

17. Program logic for programming a programmable logic device, the program logic comprising:

host interface logic for interfacing with [the] a number of host applications;

memory interface logic for interfacing with [the] a memory device wherein one or more of the host applications and the memory device have different interface requirements;

a number of contexts operably coupled to the host interface logic for receiving memory access requests from the number of host applications and providing result/status information to the number of host applications; and

control logic operably coupled to obtain memory access requests from the number of contexts, interact with the memory device using the memory interface logic for servicing the memory access requests on behalf of the number of host applications in accordance with the interface requirements for the memory device, and provide the result/status information to the number of host applications via the number of contexts in accordance with the interface requirements for each of the number of host applications.

32. An apparatus comprising:

a number of host applications;

A3

a memory device, wherein one or more of the host applications and the memory device have different interface requirements; and

a memory interface device interposed between the host applications and the memory device and operably coupled to receive memory access requests from the number of host applications, interact with the memory device on behalf of the number of host applications for servicing the memory access requests in accordance with the interface requirements for the memory device, and provide result/status information to the host applications in accordance with the interface requirements for each of the number of host applications.

Remarks

Claims 1, 17 and 32 have been amended. Claims 1-48 are pending in this Application. Reconsideration and re-examination of this application is respectfully requested in view of the following remarks.

Claim Rejections – 35 U.S.C. § 102

Claim 32 has been rejected under 35 U.S.C. 102(b) as being anticipated by Bauman et al. (US patent no. 5,875,472). This rejection is respectfully traversed.

Applicant's claim 32 recites:

"An apparatus comprising:
a number of host applications;
a memory device, wherein one or more of the host applications and the memory device have different interface requirements; and